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Designing an Efficient Rail-to-Rail Class AB Amplifier as Buffer In LCD

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ABSTRACT

For enhancing the high color depth and to provide higher resolution for LCD signal driver. This paper proposes a complementary differential amplifier with offset voltage cancellation technique. In order to improve the offset cancellation ability the complementary differential pairs are separated into main and auxiliary transconductance amplifiers. This achieves Rail-to-Rail output swing. In the proposed method offset cancellation is achieved by dividing offset cancellation and driving phases with the help of three switches. With this proposed architecture the offset voltage is reduced from 8.9 mV to 0.3 mV, which is a considerable amount of reduction. It is also observed that CMRR and Slew rate are not affected with the proposed technique

Key words: LCD, Amplifier, Signal driver, Rail-to-Rail.

INTRODUCTION

With increasing demand of LCD panel for high color depth and resolution it is hard to design a buffer with high resolution. The buffer has to match the speed, resolution, voltage swing and power dissipation of an LCD driver's to get high resolution. The resolution of the amplifier is dependent on the settling time the offset voltage and the slew rate.

The offset voltage is caused by the mismatch of the devices used in the circuit which limits the high-resolution of LCD driver. The general technique used to reduce the offset voltage is the output offset storage technique and input offset storage technique. However these two techniques introduce capacitors in the signal flow path. This is a serious issue in operational amplifiers and feedback systems. Parasitic capacitors thus formed can cause degradation of phase margin of the circuit thereby reducing stability of the circuit. So we have to design a circuit in such a manner that the offset cancellation technique should not come in the way of signal flow path.

We generally design a buffer with push-pull output stage which consists of two complementary common source transistors allowing RAIL TO RAIL output voltage swing. The gates of two output transistors can be driven by two in phase AC signals

separated by DC voltage. In this paper single ended amplifiers are used to drive the two output devices to achieve offset cancellation and to drive push-pull output. We use class AB operation because no extra current paths are needed in this operation.

The equivalent circuit of the proposed two-stage amplifier is shown in Fig.1, where g_{m1} and g_{m2} , R_{01} and R_{02}, and C_{01} and C_{02} are the transconductances, output resistances, and output parasitic capacitances of the first-stage and second-stage amplifiers, respectively. C_{CS} and R_{CS} are used for the stability of the circuit. The data line of the LCD panel is an R-C distribution. To simplify the small-signal analysis, the data line is modeled as a first-order R-C circuit. Since the first stage amplifier contains dual complementary differential pairs, the value of g_{m1} depends on the input common-mode voltage.

Design issues

To evaluate this value of g_{m1} ,the input voltage is divided into low, middle, and high levels. When the input voltage is at the low level, the PMOS input transconductance amplifiers are operating and the NMOS input transconductance amplifiers are cut off, *vice versa* for the high-level inputs. All transconductance amplifiers can amplify the input signal when the input voltage is at the middle level. Hence, the value of g_{m1} can be expressed as

$$g_{m1}=g_{mn}+g_{man} \quad ...(1A)$$

As the input voltage is at high-level;

$$g_{m1}=g_{map}+g_{mn}+g_{mp}+g_{man} \quad ...(1B)$$

As the input voltage is at the middle level;

$$g_{m1}=g_{map}+g_{mp} \quad ...(1C)$$

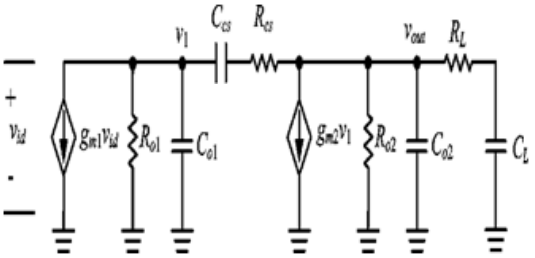

Fig. 1: Small signal equivalent circuit of the Proposed two-stage amplifier

As the input voltage is at a low level in equation (1) where $g_{man,}$ g_{mp}, g_{map}, g_{mn} are the transconductance amplifiers G_{map}, G_{mn}, G_{man}, G_{mp} respectively. Since the transconductance of the first stage amplifier varies with the input common-mode voltage, the dc gain of the amplifier varies over the signal swing for large signals. The distortion will then be generated in a continuously large signal. To reduce the distortion encountered due to this variation, the input stage should be modified to a rail-to-rail constant *gm* differential amplifier. For an LCD driver application, the amplifier is used to buffer the step-wise signals. Hence, the constant *gm* design is not suitable.

The open-loop transfer function $A_O(s)$ can be obtained from Fig. 2 and the assumptions:

$$C_{01}, C_{01} < C_{cs} < C_L; R_{01}, R_{02} > R_{cs}, R_L; \text{and } g_{m2}R_L \ll 1 \text{ that is}$$

$$A_0(s) = \frac{V_{out}(s)}{V_{id}(s)} \quad ...(2A)$$

$$= A_{dc}\frac{\left(1+\frac{s}{w_{z1}}\right)\left(1+\frac{s}{w_{z2}}\right)}{\left(1+\frac{s}{w_{p1}}\right)\left(1+\frac{s}{w_{p2}}\right)\left(1+\frac{s}{w_{p3}}\right)\left(1+\frac{s}{w_{p4}}\right)} \quad ...(2B)$$

Where

$$A_{dc} = g_{m1}g_{m2}R_{01}R_{02}$$

and

$$w_{z1} = \frac{1}{C_L R_L}$$

$$w_{z2} = \frac{1}{C_{cs}(R_{cs} - 1/g_{m2})} \quad ...(3)$$

$$w_{p1} \cong \frac{1}{C_{cs}(g_{m2}R_{02})R_{01} + C_L R_{02}} \quad ...(4)$$

$$w_{p2} \cong \frac{C_L + C_{cs}g_{m2}R_{01}}{C_L R_{01} C_{cs}} \quad ...(5)$$

$$w_{p3} = \frac{1}{C_{01}(2R_L - R_{cs})} \quad ...(6)$$

$$w_{p4} = \frac{2R_L + R_{cs}}{C_{02}R_L R_{cs}} \quad ...(7)$$

The zeros at w_{z1} and w_{z2} are contributed by the distributed load and the Miller compensation, respectively. The dominant pole w_{p1} , is due to the Miller compensation and the distributed R-C load. The first term of the denominator in (4) is arisen at the interface between the first and second stages. The output resistance of the first stage,R_{01}, is interacting with the Miller capacitance,$C_{CS}g_{m2}R_{02}$ at the interface. The second term is due to the output resistance of the second stage and the load capacitance. Since the load capacitance of the LCD data line can be the order of hundred pico-farads, the second term,$C_L R_{02}$, cannot be neglected in the LCD driver application.

The second non-dominant pole w_{p2} is arisen at the output of the second stage amplifier with the Miller effect. For a conventional two-stage operational amplifier, the first term of the numerator in (5) is much smaller than the second one, resulting to that

$$w_{p2} = {g_{m2}}/{C_L} \quad ...(8)$$

That is: w_{p2} is determined by the trasnconductance of the second stage amplifier and the load capacitance. Here, for the LCD driver application, the load capacitance cannot be neglected. If is much greater than $C_{CS}g_{M2}R_{01}$, w_{p2} can be approximately expressed as: $1/C_{CS}R_{01}$, which is independent on the transconductance of the second stage amplifier and the load capacitance.

The third and fourth nondominant poles w_{p3} and w_{p4} due to the parasitic capacitances, are far away from the other poles and zeros. Hence, they have less effect on the stability. The unity-gain frequency can be approximately expressed as

$$w_t = A_{dc}w_{p1} \cong \frac{g_{m1}g_{m2}R_{01}R_{02}}{C_{cs}g_{m2}R_{02}R_{01} + C_L R_{02}} \quad ...(9)$$

which is larger than the second pole

Hence, the actual value of the unity-gain frequency is slightly smaller than that of (8). The position of w_{z1} is greatly affected by the R-C load. The larger the load connected to the amplifier, the smaller the value of w_{z1} decreasing to less than the unity-gain frequency for a large load.

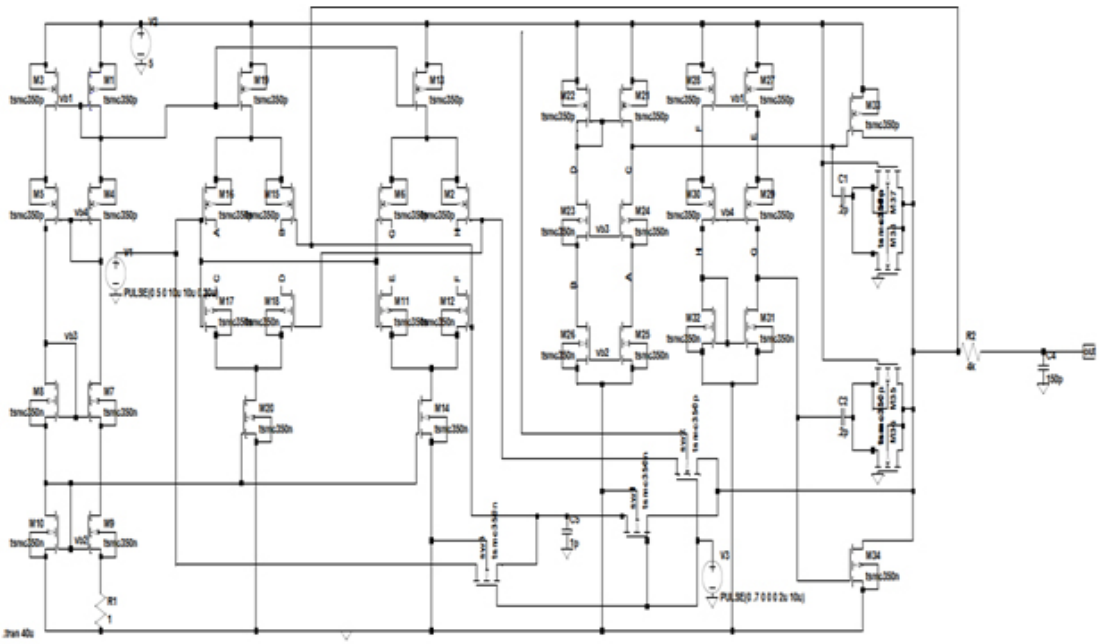

Fig. 2: Schematic of proposed buffer with offset cancellation using LTSpice

Proposed amplifier design

The auxiliary transconductance amplifiers are used to extend the input swing. They can also be used for the offset cancellation. The architecture of the proposed amplifier without an offset cancellation is shown in Figure 2, and The architecture of the proposed amplifier with an offset cancellation is shown in Fig 4.4 where an offset storage capacitor and three switches are used in the circuit, andV_{OS1}, V_{OS2}, V_{OS3} and V_{OS4} are the input-referred offset voltages of G_{map}, G_{mn}, G_{man}, G_{mp} respectively.

Since the input stage contains both PMOS and NMOS differential amplifiers, the offset voltage varies with the input voltage. For the LCD driver application, a step-wise signal is applied to the input of the buffer amplifier. Hence, the buffer amplifier must sample each voltage level for the offset cancellation. The operation is divided into offset cancellation and driving phases. Before each driving phase, the amplifier is in the offset cancellation phase, the switches SW2 and SW3 are turned on, and the switch SW1 is turned off. After the offset cancellation is finished, SW1 is turned on and SW2 and SW3 are turned off. The circuit is then ready to drive its load.

During the offset cancellation phase, a negative feedback loop consisting of the auxiliary transconductance amplifiers, G_{map} and G_{man} the transimpedance amplifiers, R1 and R2, and the output transistors, M25 and M26, is formed. The input voltage is applied to the inverting input terminals of all transconductance amplifiers and to the non-inverting input terminals of the two main transconductance amplifiers. As depicted in Fig. 3, the input-referred offset voltages V_{OS1} and, V_{OS2} are applied to the two inputs of G_{mn} and G_{mp} , respectively. The relation between the input and output voltages can be expressed as

$$\left\{\begin{matrix}[\pm V_{OS1}g_{mn} + (V_{out} - V_{in} \pm V_{OS3})g_{map}]R_1 g_{m25} \\ +[\pm V_{OS2}g_{mp} + (V_{out} - V_{in} \pm V_{OS4})g_{man}]R_2 g_{m26}\end{matrix}\right\} R_{out} = V_{out}$$

...(10)

where g_{m25} and g_{m26} are the transconductances of M25 and M26, respectively, and R_{out} is the output resistance of the amplifier. assume $g_{m25} = g_{m26}$ and $R_1 = R_2$ then

$$V_{out} = \frac{\left[\begin{matrix}V_{in}(g_{map}g_{m25}R_1 + g_{man}g_{m26}R_2) \pm \\ (V_{OS1}g_{mn} + V_{OS3}g_{map})g_{m25}R_1 \pm \\ (V_{OS2}g_{mp} + V_{OS4}g_{man})g_{m26}R_2\end{matrix}\right] R_{out}}{(g_{map}g_{m25}R_1 + g_{man}g_{m26}R_2)R_{out} - 1}$$

$$\cong V_{in} + \frac{\begin{matrix}\pm V_{OS1}g_{mn}g_{m25}R_1 \pm V_{OS2}g_{mp}g_{m26}R_2 \\ \pm V_{OS3}g_{map}g_{m25}R_1 \pm V_{OS4}g_{man}g_{m26}R_2\end{matrix}}{g_{map}g_{m25}R_1 + g_{man}g_{m26}R_2}$$

...(11)

assume $g_{m25} = g_{m26}$ and $R_1 = R_2$ then

$$V_{out} \cong V_{in} + \frac{\begin{matrix}\pm V_{OS1}g_{mn} \pm V_{OS2}g_{mp} \\ \pm V_{OS3}g_{map} \pm V_{OS4}g_{man}\end{matrix}}{g_{map} + g_{man}}$$

...(12)

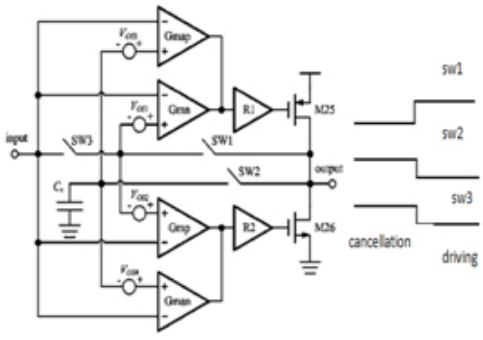

Fig. 3: Proposed amplifier with offset cancellation

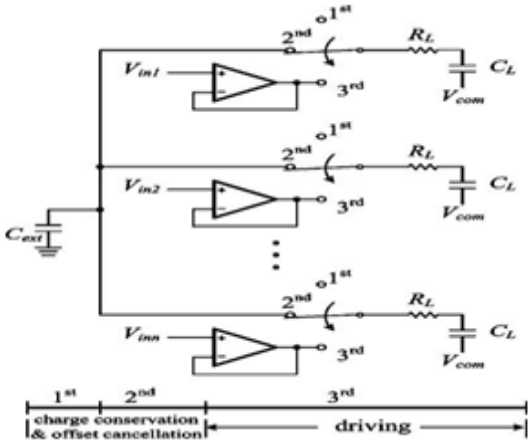

Fig. 4: Diagram of charge conservation technology

When SW2 andSW3 were off and SW1 is on the output voltage is stored at the capacitance called as output offset voltage is

$$V_{out} - V_{in} \cong \frac{\pm V_{OS1} g_{mn} \pm V_{OS2} g_{mp}}{\pm V_{OS3} g_{map} \pm V_{OS4} g_{man}} \\ g_{map} + g_{man}$$

...(13)

The total output of the voltage referred to the input is given as

$$V_{OS,tot} = \frac{V_{out} - V_{in}}{A_{dc}} = \frac{\pm V_{OS1} g_{mn} \pm V_{OS2} g_{mp}}{\pm V_{OS3} g_{map} \pm V_{OS4} g_{man}} \\ (g_{map} + g_{man}) A_{dc}$$

...(14)

Where A_{DC} is the DC gain of amplifier of the order of 80 dB. The switch SW2 will introduce injection induced either with generate, input referred offset voltage expressed as

$$V_{OS,inj} = \left(\frac{g_{map} + g_{man}}{g_{mn} + g_{mp}} \right) \Delta V$$

...(15)

Where "V is the injection induced error on the storage capacitor to reduce the center the transconductance of the main transconductance amplifier is designed to be higher than auxiliary transconductance amplifier. In this methodology charge conservation technology is used to reduce the power consumption. In this process the data line are divided into three phase as in first phase all data lines are isolated from the output of the buffers. In second phase they are shorted with external capacitor, this two phases are used to conserve charge on data line in last phase all data lines connected with output buffer to drive the data line to their final values. This charge conservation is used for offset cancellation, and it eliminates the need of additional phase consideration for the buffer amplifier means the driving time does not need to be elongated.

Charge conservation technology, which is shown in Fig.4, is usually used to reduce the power consumption by reducing the average voltage swing. The voltage level refresh of the data lines is divided to three phases. In the first phase, all data lines are isolated from the outputs of the buffers. In the second phase, they are shorted to an external capacitor C_{ext}. These first two phases are used for the charge conservation of the data lines. In the last phase, all data lines are connected to their corresponding buffer amplifiers, and the buffer amplifiers continue to drive the data lines to their final values. The charge conservation phase can also be used for the offset cancellation of the proposed amplifier, eliminating the need for an additional phase for offset cancellation. Thus, the driving time does not need to increase.

Design process of buffer

(A) Design Process (1/3)

Model Parameter Extraction

- kn ,kp
- λn ,-λp
- Vthn ,Vthp

all these can be get by process technology

Assign Current from Power Consumption Spec.

- Total Current : 3I mA
- Input pair : I mA
- Current mirror : 2I mA

(B) Design Process (2/3)

.Determine W3 from CM_min, CM_max Spec.

- CM_min

Table 1: Aspect Ratio of Buffer

M1=3u/2u	M9=(4	M17=3u/2u	M25=(4
M2=(2	M10=(2	M18=3u/2u	M26=(2
M3=(2	M11=(2	M19=3u/2u	Mr1=1u/7u
M4=(4	M12=3u/2u	M20=3u/2u	Mr2=1u/7u
M5=(4	M13=(2	M21=3u/2u	Mr3=1u/7u
M6=3u/2u	M14=(2	M22=3u/2u	Mr4=1u/7u
M7=3u/2u	M15=3u/2u	M23=3u/2u	Ccs1=.2pF, Ccs1=.2pF
M8=(4	M16=3u/2u	M24=3u/2u	Cs=1pF

$V_{SS} + V_{DSAT3} + V_{GS1} = V_{SS} + V_{DSAT3} + V_{DSAT1} + V_{THn1}$

- CM_max $V_{DD} - |V_{DSAT4}| + V_{THn1}$

Determine W4~W7 and Bias2 from Vout_max Spec.

- Vout_max : $V_{B2} + |V_{THP7}|$ Determine VB2

- Assign Vdsat of M4,5 and M6,7 from Vout_max Spec

Eg: Vout_max=4V '!Vdsat of M4,5= 0.6V, Vdsat of M6,7 = 0.4V

- Calculate W4~7 to satisfy Vdsat & Ids of M4~7

Determine W8~W11 from Vout_min Spec.

- Assign Vdsat of M8~M11 from Vout_min Spec.

Eg) Vout_min=0.8V '!Vdsat of M8~11 = 0.4V

- Calculate W8~11 to satisfy Vdsat and Ids of M8~11

Design Process (3/3)

.Determine W1,2 from Gain Spec.

$$R_0 = \frac{V_X}{i_X} = \{g_m r_{07} \cdot (r_{02} || r_{05})\} || \{g_{m9} r_{09} \cdot r_{011}\}$$

- Calculate Required Gm value to satisfy Gain Spec.

.Gain = Gm*Rout

- Calculate W1,2 from Gm

.Check other Spec. and Repeat the design process to optimize

transistors size

- Slew Rate

- CM_min Check required

- CMRR, PSRR

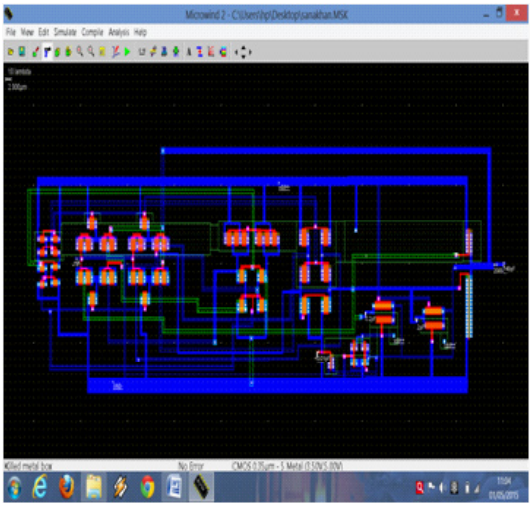

Fig. 5: Layout of the implemented buffer

- Check and Modify Bias Voltage to optimize transistor size.

RESULTS

Simulation and results are obtained using LTSPICE & MICROWIND software's. Results illustrate the tracking behavior of the proposed output buffer driven by a 50-kHz large-swing triangular wave and loaded with a large-size capacitance of 140pF. As can be inspected, the output voltage basically follows the input voltage for a full dynamic range. To show the output driving performance of the discussed buffer, results depicts the simulated transient response to a 50-kHz full-swing input step for the same capacitive load. Slew-rate values are found to be 12V/µs and 14V/µs for the rising and falling edges, respectively, whereas positive and negative settling time values within 1000% of the final output voltage are only 3µs and 3.7µs, respectively. As can be observed, the output waveform follows the input waveform. The major performance parameters of the analyzed buffer are summarized and compared to other conventional topologies in Table 5, which shows a remarkable improvement of the proposed amplifier over other

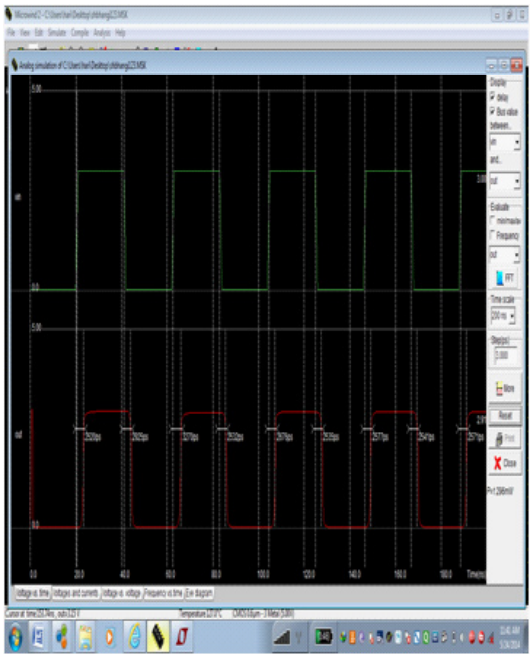

Fig. 6: Input and output waveforms of the voltage

Table 2: Comparison Table For Offset Voltage Value

Offset value without switches	Offset voltage with 3 switches
8.9 mV	0.3 µV

Table 3: Comparison Table for CMRR(Common Mode Rejection Ratio)

CMRR without switches	CMRR with 3 switches
$10^{11.2}$	$10^{11.27}$

Table 4: Comparison Table For Slew Rate

Slew rate without switches	Slew rate with 3 switches
4.5/2.4 V/µs	4.5/2.4 V/µ

previously reported buffers. Figure 5 shows the layout of the analog buffer manually designed using Microwind. And the next diagram figure 6 shows its timing diagram. We can clearly see that output follows input. Table 2 compares the offset values using offset cancellation technique and without it. The method used for this work makes a huge difference in the offset voltage value. Similarly Tables 3 and 4 show that the inclusion of the three switches does not affect the CMRR and Slew Rate values.

Table 5: Comparison Table

	[12] IQ Ito's Amplifier	[13] Weng's Amplifier	[14]Hong's Amplifier	This work
Process technology	.35 µm CMOS	.35 µm CMOS	.35 µm CMOS	.35 µm CMOS
VDD	5 V	3.3 V	5 V	5 V
Input-output range	0.5-4.5 V	.05-3.25 V	0-5 V	0-5V(100% VDD)
Quiescent current	2 µA	7.4 µA	NA	7 µm
DC gain	NA	65db	NA	88db
Unity gain frequency	NA	750KHz	NA	3.5 MHz
Phase margin	NA	50	45	109
Settling time	1.95 µs (24 Pf Load)	8 µs (600pF Load)	.95 µs (400pF Load)	3 µs (140pF Load)
Offset voltage	NA	NA	N	.3 mV
Active area	100*46µm²	100*100 µm²	86*74 µm²	100*50 µm²

CONCLUSION

It is limpidly visually perceived in the results that the output waveform follows the input waveform. Withal the comparison table depicts a remarkable amelioration of the proposed amplifier over other antecedently reported buffers. Hence the high speed self inequitable low power rail-to-rail class-AB low offset buffer amplifier is implemented prosperously, Since the dissertation topic implements a very compact, high speed rail-to-rail buffer for LCD drivers, it can be utilized as a boon in many future applications where die area is a matter of concern, additionally where slew rates is a matter of concern. Since it utilises a only 0.74 mV of static puissance, hence is having tremendous demand in hundreds of exhibit contrivances applications.

Due its merits, it can be utilized in following areas-

- Since power consumption is low, it has a great future in getting utilized in applications like "ultra low power ADCs".
- Since it is utilizing AMLCD technology, the exhibit is amended remarkably, hence can be utilized in "image exhibit contrivances, flat

panel exhibits etc.

- Due to rail-to-rail input and output cognations, it is greatly utilized in buffered analog clocks .Above are just few examples, but this buffer is having excellent usability in many other areas also.
- As with reduced offset it will be use full for high colour depth LCD panels means resolution of colour will increase significantly

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