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What Causes to Tune a Condition of Exactly Identical Fault-Masks Behaviors in an LFSR based BIST Methodology

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Abstract

The authors show that in a Built-In Self-Test (BIST) technique, based on linear-feedback shift registers, when the feedback connections in pseudo-random test-sequence generator and signature analyzer are images of each other and corresponds to primitive characteristic polynomial then behaviors of faults masking remains identical. The simulation results of single stuck-at faults show how the use of such feedback connections in pseudo-random test-sequence generator and signature analyzer yields to mask the same faults.

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Linear Feedback Shift Register, Characteristic Polynomial, Test Pattern, Built–In Self-Test, Pseudo-Random Test Sequence Generators, Signature Analyzer

Introduction

In recent years, numerous Built-In Self-Test (BIST) systems have been proposed just because of its gaining acceptance in the VLSI industry due to its popular enormous advantages[1–6].With BIST methodology, there is no need to use external test equipment sincea self-testable circuitry is built on the chip itself. The BIST technique usually combines a built-in Pseudo-Random Test-Sequence (PRTS) generation with an output response analyzer. This methodology relief us from the complex task of test-sequence generation and decreases the storage requirements of test-sequences and response data. Since, in BIST methodology, test-signals are applied using normal clock rate, therefore, testing of a chip that designed with BIST methodology can be performed at-speed. Additionally, because the test resources are available during the entire life of the chip, thus, diagnosis and maintenance of the systems can be greatly simplified.

Figure 1 depicts a general Linear Feedback Shift Registers (LFSRs) based test model for BIST technique. In particular, PRTS generation followed by the compression of response data by Signature Analyzer (SA) has become a standard form of testing

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technique in BIST environment. LFSRs are usually used in this form of testing in both Pseudo-Random Test-Sequence Generators (PRTSGs) as well as in SAs. Undoubtedly, LFSR-basedPRTS generation is known to be an extremely simple method of generating a required number of test-sequences. Although, various estimation and trade-off schemes have been floated to determine the length of the test-sequences that will be required to achieve the desired fault coverage. However, these schemes usually give a number that is only an estimate and sometimes too large. To overcome these problems, a 'divide-and-conquer' approach for testing of large sizes of circuits has been proposed[7–15]. The philosophy behind the divide-and-conquer approach of testing is to apply either the exhaustive test-stimuli or maximal length PRTSs to the different segmented units of the Digital Circuit Under Test (DCUT).

An added difficulty arises when the resulting circuit response data is compressed into small signature using the SA. Although, the signature analysis scheme which is easily implemented by LFSRs, but it leads to loss of information, due to the erroneous response patterns that get compressed into the same signature as the fault-free signature. Thus, some of the faults might go undetected due to this fault-masking phenomenon and resulting to reduce the fault coverage of the DCUT. A Method to determine the extent of fault masking and its phenomenon in any DCUT is not readily available. However, many approaches have been suggested[1–22] to analyze and improve the basic signature analysis schemes. The use of primitive polynomials in SA with some restrictions[7,15,17,20–22] along with obtaining multiple signatures with the use of different feedback connections in LFSRs of PRTSG as well as of SA [1,3-5,18,19] can prove a better solution for minimizing the fault-masks.

Thus, in LFSR based BIST test methodology, to achieve better fault coverage for a DCUT the following suggestions have been given by the researchers.

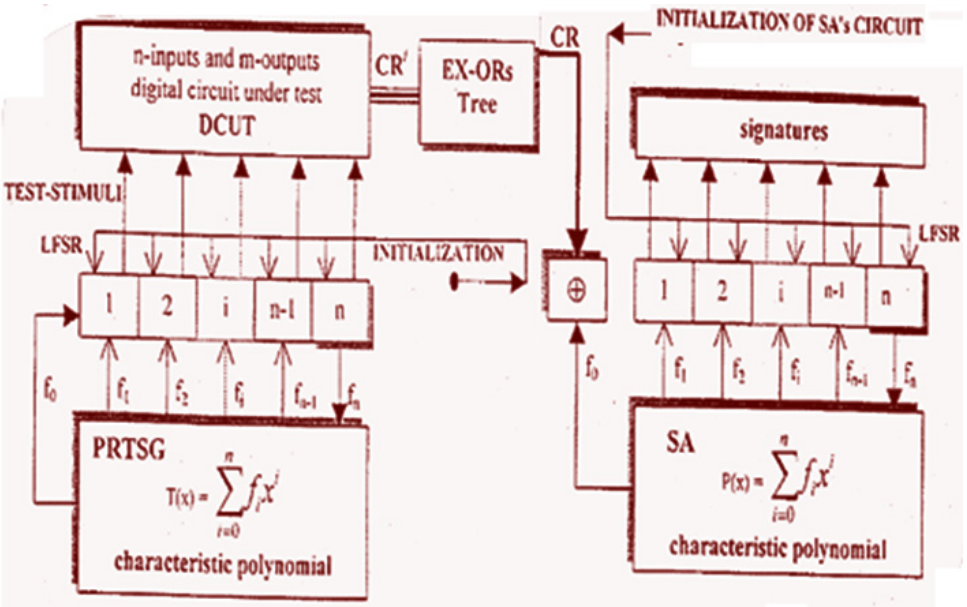

Fig.1: The testing model of an LFSR based BIST technique

- Use of those feedback connections in PRTSGs, which correspond to primitive polynomials to generate maximal length PRTSs.
- Use of those feedback connections in SAs, which correspond to primitive polynomials.
- Use of multiple feedback connections in the LFSRs of PRTSG as well as of the SA.

However, this paper reports and demonstrates an interesting and peculiar result of a simulation study of an LFSR based testing technique where the

feedback connections of LFSRs used in PRTSG as well as of SA correspond to primitive polynomials of order n, for an n-input DCUT. It is investigated through the compiled results of this study that when the feedback connections of PRTSs and of SAs are images of each other than behaviors of faults masking remains identical and hence, not enhancing the fault coverage due to the changes of the feedback connections.

Simulation Experiment

The testing model employed in our simulation experiment is the same as the standard BIST models used in the studies[1-22]. The BIST standard model is shown in Figure 1. Various n-input combinational circuits summarized in Table I, have been simulated using the referred IC's manufacturer's logical diagrams with gate level description. In the simulation procedure, to get the single bit stream of circuit response (CR) from multiple output circuits, an appropriate tree of Exclusive-ORs is used.

Table 1: Summary Of Simulated Circuits. Cn: Circuit Number; Cs: Circuit Specification; Nfi: Number Of Faults Injected; Npi: Number Of Possible Feedback Connections Corresponding To Primitive Polynomials

CN	IC No.	CS	NFI	NPI
CN-1	SN74LS139	3-input 58 4-outputs 9 gates	2	
CN-2	SN74LS139	3-input 90 2-outputs 12 gates	2	
CN-3	SN74LS145	4-input 10-outputs 18 gates	180	2
CN-4	SN74LS82	5-input 3-outputs 21 gates	148	6
CN-5	SN74H87	6-input 4-outputs 14 gates	64	6
CN-6	SN74LS138	6-input 8-outputs 19 gates	154	6
CN-7	SN74LS352	7-input 1-outputs 10 gates	70	18
CN-8	SN74LS283	9-input 5-outputs 36 gates	252	48
CN-9	SN74LS280	9-input 2-outputs 46 gates	294	48

A single stuck-at fault model is assumed where s-a-0 and s-a-1 faults are postulated on each individual connecting lines (out of the total number, NC), of the DCUT. Each possible image pairs of feedback connections (F, FI) as described by Equations (1) and (2) are used in the simulation.

$$F = \{f_{i0}, f_{i1}, f_{i2}, \ldots, f_{ij}, \ldots, f_{i(n-1)}, f_{in}\} \quad ...(1)$$

$$F_I = \{f_{i0}, f_{i(n-1)}, f_{i(n-2)}, .., f_{i(n-j)}, \ldots, f_{i(n-n+1)}, f_{in}\} \quad ...(2)$$

The feedback connections (F, F_I) correspond to primitive polynomials of order n (out of the set of the total such possible feedback connections, $NFB = 2^{n-1}; 1 \leq i \leq NFB$), are used to equip the LFSRs of PRTSG and of SA respectively.

Finally, the simulation procedure collects the identification list of masked faults for each set of image pairs of feedback connections of LFSRs. For the study of an n-input combinational circuit, the adopted formal procedure to compile the list of identified masked faults for each set of image pairs of feedback connections of LFSRs, is summarized in the form of an algorithm and is given below:

Algorithm
(For a circuit segment's unit under test having an n-input).

Step 0
Choose the i^{th} (i = 1 to NFB) feedback connection (fi0 , fi1 , . . . , fij , . . . , fi(n-1) , fin) for the LFSRs used in PRTSG (say; FBTI) such that it corresponds to primitive polynomial.

Step 1
Generate the image of FBTI and equip the LFSRs of SA with these feedback connections (say; FBSI).

Step 2
Load LFSR used in PRTSG with initial state (other than all 0s initial state vectors).

Step 3
Generate PRTS of length 2^{n-1}.

Step 4
Evaluate DCUT's response CR_k (k = 0 to 2 NC).

Step 5
Load LFSR used in SA with initial state (all 0s).

Step 6
Choose DCUT's response CR_k (CR_0 is fault-free response, CR_1 is the response under condition when connecting line #1 is subjected to s-a-0 fault, CR_2 is the response under condition when connecting line #1 is subjected to s-a-1 fault. Similarly, CR_3 is the response under condition when connecting line #2 is subjected to s-a-0 fault and CR_4 is the response under condition when connecting line #2 is subjected to s-a-1 fault etc. respectively).

Step 7
Compute signature S_k

Step 8
Check faults masks, if the k^{th} fault is masked, update the faults masks list by adding the k^{th} fault.

Step 9
Obtain the faults masks list for each set of FBTI and FBSI.

Step 10
Print the list of masked faults.

Study
Using the above-mentioned procedures, we compiled the list of the masked faults for each circuit of our simulation study. Tables II shows one of such simulation results for circuit CN-1 (refer to manufacturer's logical diagram as shown in Figure2).

It is noted that in a 3-bit LFSR, the number of those possible feedback connections which correspond to primitive polynomials is two, and they are (f_0, f_1, f_3) and (f_0, f_2, f_3). The feedback connections (f_0, f_1, f_3) and (f_0, f_2, f_3) are images of each other. It can be seen from the table that when the feedback connections of PRTSG and of SA are (f_0, f_1, f_3) and (f_0, f_2, f_3) respectively, which is image of each other, then the identified masked faults are c1/0, c1/1, c2/0, c2/1, c3/0, c3/1, c4/0, c4/1, c5/0, c5/1, c6/0, c6/1, c26/0.

Further, it can also be observed from the results of the same table, that exactly the same faults are being masked when we use (f_0, f_2, f_3) and (f_0, f_1, f_3) as feedback connections in PRTSG and SA respectively. Also, another simulation result is presented here in Table III, which is obtained for CN-2 (see Figure 3).

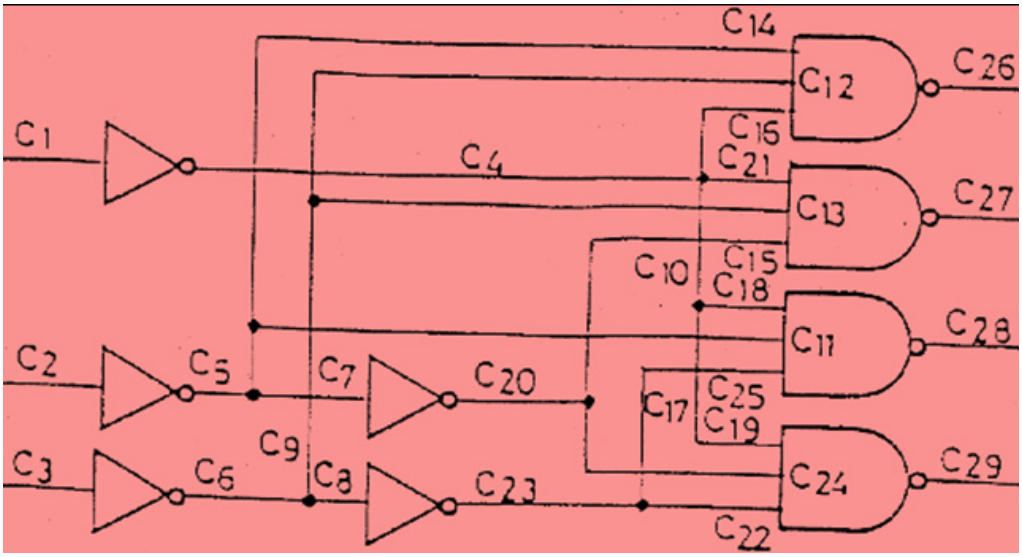

Fig. 2: Logic diagram of CN-1

Table 2: Circuit Cn-1; Figure 2

Feedback connections used in LFSRs of PRTPG / SA	List of masked faults (s-a)
(f_0, f_1, f_3) / (f_0, f_2, f_3)	$c_1/0$, $c_1/1$, $c_2/0$, $c_2/1$, $c_3/0$, $c_3/1$, $c_4/0$, $c_4/1$, $c_5/0$, $c_5/1$, $c_6/0$, $c_6/1$, $c_{26}/0$
(f_0, f_2, f_3) / (f_0, f_1, f_3)	$c_1/0$, $c_1/1$, $c_2/0$, $c_2/1$, $c_3/0$, $c_3/1$, $c_4/0$, $c_4/1$, $c_5/0$, $c_5/1$, $c_6/0$, $c_6/1$, $c_{26}/0$

Table 3: Circuit Cn-2; Figure 2

Feedback connections used in LFSRs of PRTPG / SA	List of masked faults (s-a)
(f_0, f_1, f_3) / (f_0, f_2, f_3)	$c_4/0$, $c_4/1$, $c_6/0$, $c_6/1$, $c_8/0$, $c_8/1$, $c_{10}/0$, $c_{10}/1$, $c_{19}/0$, $c_{19}/1$, $c_{28}/0$, $c_{28}/1$, $c_{40}/1$, $c_{41}/1$, $c_{42}/1$, $c_{43}/1$, $c_{45}/0$, $c_{45}/1$
(f_0, f_2, f_3) / (f_0, f_1, f_3)	$c_4/0$, $c_4/1$, $c_6/0$, $c_6/1$, $c_8/0$, $c_8/1$, $c_{10}/0$, $c_{10}/1$, $c_{19}/0$, $c_{19}/1$, $c_{28}/0$, $c_{28}/1$, $c_{40}/1$, $c_{41}/1$, $c_{42}/1$, $c_{43}/1$, $c_{45}/0$, $c_{45}/1$

In the interest of space, we presented the simulation results for only two circuits, but our findings are similar for other circuits of our simulation study as well. In addition, we simulated many more randomly selected circuits and observed the same results.

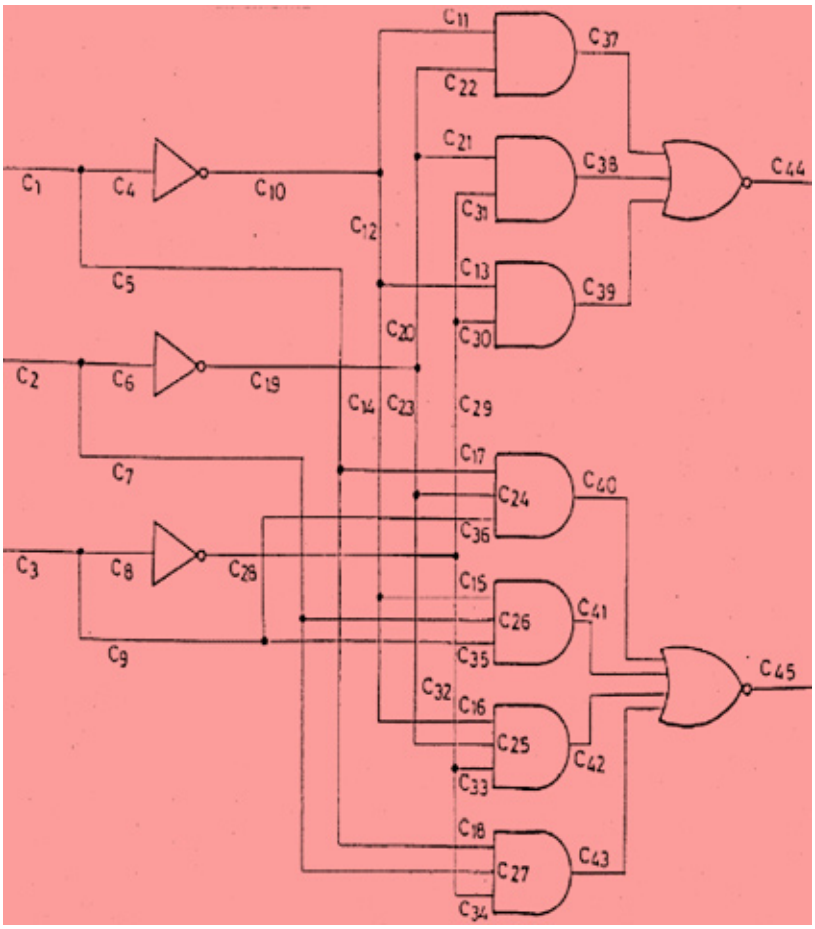

Fig.3: Logic diagram of CN-2

Conclusion

We have shown that when we use such linear maximal sequence generator in test pattern generation whose feedback connections are images of feedback connections of signature analyzer and corresponds to primitive characteristic polynomial then behaviors of faults masking remains identical. The results demonstrate that how the use of such feedback connections in pseudo-random test-sequence generator and signature analyzer yields to mask the same faults. These results are based on the simulation study of single stuck-at faults.

Thus, although maximal length pseudo-random binary-test sequences are the best ones for pseudo-exhaustive testing environment. However, this objective can only be achieved by proper selection of feedback connections of pseudo-random binary-test sequence generator as well as of signature analyzer. This identical fault mask behavior observed throughout this simulation study leads to the fact that the test schemes based on linear feedback shift registers need to be analyzed in totality instead of separately analyzing the LFSRs of either PRTSG or of SA to achieve higher fault coverage.

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